Amendments to the Claims

Please amend the claims in the manner indicated:

1. (currently amended) A method to order memory operations in a multi-processor system, the method comprising:

~~using at least one signal to indicate that a particular kind of memory operation is not globally observable but is observable by at least one processor of the system~~

dividing a memory space of the system into at least two regions;

using at least two signals for each region of the at least two regions, wherein each signal of the at least two signals is associated with a particular kind of memory operation to one region of the at least two regions and indicates that the particular kind of memory operation is not globally observable in the one region but is observable in the one region by at least one processor of the multi-processor system.

2. (currently amended) The method of claim 1, ~~wherein using includes using at least two signals,~~ wherein a first signal of the at least two signals for a particular region indicates that a load operation issued by the at least one processor is not globally observable for the particular region by all processors of the system but is observable by the at least one processor for the particular region and wherein a second signal of the at least two signals for the particular region indicates that a store operation issued by the at

least one processor is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor.

3. (currently amended) The method of claim 1, further including ~~wherein using includes~~ using at least three signals for each region of the at least two regions, wherein a first signal of the at least three signals for a particular region indicates that a load operation issued by the at least one processor is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor, wherein a second signal of the at least three signals for the particular region indicates that a store operation issued by the at least one processor is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor, wherein a third signal of the at least three signals for the particular region indicates that a swap operation issued by the at least one processor is not globally observable for the particular region by all processors of the system but is observable by the at least one processor for the particular region.

4. (cancelled)

5. (currently amended) The method of claim 1, wherein said using includes using a first signal of the at least two signals to indicate that a store operation issued by the at least one processor is not globally observable for the particular region by all processors of the system.

6. (currently amended) The method of claim 5, further comprising asserting the first signal to indicate that the store operation is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor.

7. (currently amended) The method of claim 6, further comprising allowing other store operations to be issued for the particular region by any of the processors of the system if the first signal is asserted.

8. (currently amended) The method of claim 6, further comprising preventing any processor of the system to issue a memory operation other than a store operation for the particular region if the first signal is asserted.

9. (currently amended) The method of claim 6, further comprising preventing any processor of the system to issue a load operation or swap operation for the particular region if the first signal is asserted.

10. (currently amended) The method of claim 6, further comprising deasserting the first signal after the store operation is globally observable for the particular region by all processors of the system.

11. (currently amended) The method of claim 1, wherein ~~using includes using~~ a first signal of the at least two signals for a particular region indicates ~~to indicate~~ that a load

operation issued by the at least one processor is not globally observable for the particular region by all processors of the system.

12. (currently amended) The method of claim 11, further comprising asserting the first signal to indicate that the load operation is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor.

13. (currently amended) The method of claim 11, further comprising allowing other load operations to be issued for the particular region by any of the processors of the system if the first signal is asserted.

14. (currently amended) The method of claim 11, further comprising preventing any processor of the system to issue a memory operation for the particular region other than a load operation if the first signal is asserted.

15. (currently amended) The method of claim 11, further comprising preventing any processor of the system to issue a store operation or swap operation for the particular region if the first signal is asserted.

16. (currently amended) The method of claim 11, further comprising deasserting the first signal after the load operation is globally observable for the particular region by all processors of the system.

17. (currently amended) The method of claim 1, wherein ~~using includes using~~ a first signal of the at least two signals for a particular region indicates ~~to indicate~~ that a swap operation issued by the at least one processor is not globally observable for the particular region by all processors of the system.

18. (currently amended) The method of claim 17, further comprising asserting the first signal to indicate that the swap operation is not globally observable for the particular region by all processors of the system but is observable for the particular region by the at least one processor.

19. (currently amended) The method of claim 17, further comprising preventing any processor of the system to issue any memory operation for the particular region if the first signal is asserted.

20. (currently amended) The method of claim 17, further comprising preventing any processor of the system to issue a load operation, a store operation, or a swap operation for the particular region if the first signal is asserted.

21. (currently amended) The method of claim 17, further comprising deasserting the first signal after the swap operation is globally observable for the particular region by all processors of the system.

22. (cancelled)

23. (currently amended) ~~The system of claim 22, further~~ A system, comprising:

a first processor;

a second processor coupled to the first processor;

a first signal line coupled to the first processor and the second processor to indicate whether a load operation is globally observable in a first region of a memory shared by the first and second processors; and

a second signal line coupled to the first processor and the second processor to indicate whether a store operation is globally observable in the first region ~~; and~~

~~a third signal line coupled to the first processor and the second processor~~.

24. (currently amended) The system of claim 23, wherein the first processor has logic to assert the first signal line after the first processor issues [[a]] the load operation to indicate that the load operation is not globally observable for the first region ~~in the system~~ but is observable by at least one processor of the system.

25. (currently amended) The system of claim 24, wherein the second processor has logic to prevent the second processor from issuing a memory operation other than a load operation to the first region while the first signal line is asserted.

26. (currently amended) The system of claim 24, wherein the second processor has logic to prevent the second processor from issuing a store operation ~~or a swap operation~~ to the first region while the first signal line is asserted.

27. (currently amended) The system of claim 23, wherein the first processor has logic to assert the second signal line after the first processor issues [[a]] the store operation to indicate that the store operation is not globally observable for the first region ~~in the system~~ but is observable by at least one processor of the system.

28. (currently amended) The system of claim 27, wherein the second processor has logic to prevent the second processor from issuing a memory operation other than a store operation to the first region while the second signal line is asserted.

29-32. (cancelled)

33. (currently amended) The system of claim 23, further comprising:

a third ~~fourth~~ signal line coupled to the first processor and the second processor; and

a fourth ~~fifth~~ signal line coupled to the first processor and the second processor~~; and~~

~~a sixth signal line coupled to the first processor and the second processor~~.

34. (cancelled)

35. (currently amended) The system of claim [[34]] 33, wherein the first processor has logic to assert the ~~second~~ third signal line after the first processor issues a load

operation to a second region of the memory of the system, wherein asserting the ~~second~~ third signal line indicates that the load operation is not globally observable for the second region but is observable for the second region by the at least one processor.

36. (cancelled)

37. (currently amended) The system of claim [[36]] 35, wherein the first processor has logic to assert the fourth signal line after the first processor issues a store operation to a second region of the memory of the system, wherein asserting the fourth signal line indicates that the store operation is not globally observable for the second region but is observable for the second region by the at least one processor.

38-39. (cancelled)

40. (currently amended) The system of claim [[22]] 23, wherein the first processor and second processor are integrated together on a single silicon die.

41. (currently amended) The system of claim [[22]] 23, further comprising:
a first local cache memory coupled to the first processor;
a second local cache memory coupled to the second processor; and
a shared cache memory, wherein the shared cache memory is coupled to the first processor via the first local cache and the shared cache is coupled to the second processor via the second local cache.

42. (currently amended) A system, comprising:

first and second processors;

a memory divided into multiple regions;

at least two signal lines for each region of the multiple regions, each of the at least two signal lines coupled to first and second processors; and

~~a first processor to use at least one signal for memory consistency, wherein the at least one signal indicates that a particular kind of memory operation is not globally observable in the system but is observable by at least one processor of the system; and~~

an antenna coupled to the first and second processors;

wherein each signal line of the at least two signal lines is associated with a particular kind of memory operation to a particular one of the multiple regions and is to indicate that the particular kind of memory operation is not globally observable for the particular one of the multiple regions but is observable for the particular one of the multiple regions by at least one processor of the system.

43-44. (cancelled)

45. (currently amended) The system of claim 42, wherein the system [[is]] comprises a wireless phone.